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09/818,024	03/26/2001	Satyanarayana Nishtala	SUN-P5569-RJL	2204

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	4

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,024	NISHTALA, SATYANARAYANA	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-8,10,11,13-15,17,18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-8,10,11,13-15,17,18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 4, 6-8, 10, 11, 13-15, 17, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greiner, U.S. Patent Application Publication U.S. 2002/0157062 in view of Rodriguez, U.S. Patent Application Publication U.S. 2002/0087921.

3. Referring to claim 1, Greiner discloses an apparatus for detecting errors on a multi-pumped bus (See page 1, paragraph 2), this is interpreted as a source synchronous bus (See page 4, paragraph 58). The source synchronous bus has a plurality of data lines, a clock line (the strobe lines are interpreted as a clock line for the source synchronous bus), a transmitting mechanism, a receiving mechanism, and an error detecting mechanism (See Fig. 5b). Greiner teaches the parity circuit checking for errors (See page 2, paragraph 29). Greiner teaches a grouping mechanism with the transmitting mechanism configured to group the data bits into error groups and a detection code generating for each group. Greiner teaches data groupings and parity outputs created for each grouping (See page 10, paragraph 115). Greiner also discloses that the detection code being transmitted using a clock cycle other than the

clock cycles for transmitting the data (See page 10, paragraph 122). Greiner discloses the data bits being skewed across time, he teaches the data group being split up among the phases of the transmission (See page 10, paragraph 115). Greiner does not disclose that the error detecting mechanism can detect errors caused by an error on the clock line, however Greiner does disclose increasing the bus throughput by increasing the rate to higher frequency. Rodriguez teaches detecting errors in a source synchronous bus that has strobe logic containing glitch detection for the strobe or "bus clock" line (See Fig. 1 and page 2, paragraph 21). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the strobe logic of Rodriguez with the source synchronous bus of Greiner. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it increases the reliability, especially for problems that are prone to high-speed connections (See Rodriguez, page 1, paragraph 4).

4. Referring to claims 3 and 4, Greiner and Rodriguez disclose all the limitations (See rejection of claim 1) including the detection code being a parity bit or an error correcting code (See Greiner page 1-2, paragraph 23).

5. Referring to claim 6 and 7, Greiner and Rodriguez disclose all the limitations (See rejection of claim 1) including the data bits being skewed across time. Greiner discloses the data group being split up among the phases of the transmission (See page 10, paragraph 115). Greiner teaches the data being skewed based on the position of the data bits (See page 10, paragraph 115 and Fig. 8 and 9). Greiner also

teaches a gathering mechanism with the receiving mechanism that de-skews the data bits (See Fig. 9).

6. Referring to claim 8, Greiner discloses a method for detecting errors on a multi-pumped bus (See page 1, paragraph 2), this is interpreted as a source synchronous bus (See page 4, paragraph 58). The source synchronous bus has a plurality of data lines, a clock line (the strobe lines are interpreted as a clock line for the source synchronous bus), transmitting data, receiving data, and detecting errors (See page 6, paragraphs 75 and 76). Greiner discloses grouping data bits into error groups and generating detection code for each group. Greiner teaches data groupings and parity outputs created for each grouping (See page 10, paragraph 115). Greiner also discloses that the detection code being transmitted using a clock cycle other than the clock cycles for transmitting the data (See page 10, paragraph 122). Greiner discloses the data bits being skewed across time, he teaches the data group being split up among the phases of the transmission (See page 10, paragraph 115). Greiner does not disclose detecting errors caused by an error on the clock line, however Greiner does disclose increasing the bus throughput by increasing the rate to higher frequency. Rodriguez teaches detecting errors in a source synchronous bus by detecting glitches on the strobe or "bus clock" line (See Fig. 1 and page 2, paragraph 21). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the detecting of glitches on the strobe line of Rodriguez with the method of detecting errors on a source synchronous bus of Greiner. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it increases the reliability, especially for

problems that are prone to high-speed connections (See Rodriguez, page 1, paragraph 4).

7. Referring to claims 10 and 11, Greiner and Rodriguez disclose all the limitations (See rejection of claim 8) including the detection code being a parity bit or an error correcting code (See Greiner page 1-2, paragraph 23).

8. Referring to claim 13-14, Greiner and Rodriguez disclose all the limitations (See rejection of claim 8) including the data bits being skewed across time. Greiner discloses the data group being split up among the phases of the transmission (See page 10, paragraph 115). Greiner teaches the data being skewed based on the position of the data bits (See page 10, paragraph 115 and Fig. 8 and 9). Greiner also teaches gathering and de-skewing the data bits (See page 10, paragraph 115).

9. Referring to claim 15, Greiner discloses a computing system for detecting errors on a multi-pumped bus (See page 1, paragraph 2, and Fig. 1), this is interpreted as a source synchronous bus (See page 4, paragraph 58). The source synchronous bus has a plurality of data lines, a clock line (the strobe lines are interpreted as a clock line for the source synchronous bus), a processor as a transmitting mechanism, a memory unit as receiving mechanism, and an error detecting mechanism coupled to the memory unit (See Fig. 1). Greiner teaches the parity circuit checking for errors (See page 2, paragraph 29). Greiner teaches a grouping mechanism with the transmitting mechanism configured to group the data bits into error groups and a detection code generating for each group. Greiner teaches data groupings and parity outputs created for each grouping (See page 10, paragraph 115). Greiner also discloses that the

detection code being transmitted using a clock cycle other than the clock cycles for transmitting the data (See page 10, paragraph 122). Greiner discloses the data bits being skewed across time, he teaches the data group being split up among the phases of the transmission (See page 10, paragraph 115). Greiner does not disclose that the error detecting mechanism can detect errors caused by an error on the clock line, however Greiner does disclose increasing bus throughput by increasing the rate to higher frequency. Rodriguez teaches detecting errors in a source synchronous bus that has strobe logic containing glitch detection for the strobe or clock line (See Fig. 1 and page 2, paragraph 21). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the strobe logic of Rodriguez with the source synchronous bus of Greiner. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it increases the reliability, especially for problems that are prone to high-speed connections (See Rodriguez, page 1, paragraph 4).

10. Referring to claims 17 and 18, Greiner and Rodriguez disclose all the limitations (See rejection of claim 15) including the detection code being a parity bit or an error correcting code (See Greiner page 1-2, paragraph 23).

11. Referring to claim 20-21, Greiner and Rodriguez disclose all the limitations (See rejection of claim 15) including the data bits being skewed across time. Greiner discloses the data group being split up among the phases of the transmission (See page 10, paragraph 115). Greiner teaches the data being skewed based on the position of the data bits (See page 10, paragraph 115 and Fig. 8 and 9). Greiner also

teaches a gathering mechanism with the receiving mechanism that de-skews the data bits (See Fig. 9).

Response to Arguments

12. Applicant's arguments filed on 29 December 2003 have been fully considered but they are not persuasive.

13. The rejection of the claims is maintained, they have been restructured to follow the moving of the dependent claims into the independent claims.

14. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., wherein each data bit and the error code are transmitted at different times) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant argues that each data bit and error code is transmitted at different times, but in fact is claiming, "wherein data bits in the error group are transmitted at different times." This does not imply that each bit is transmitted at a different time, but that as a whole they are not transmitted at the same time. This means subsets of the whole group can be transmitted at the same time, just not all the subsets transmitted at the same time. Greiner teaches the error group being broken up in to four subsets and each being transmitted during a different phase of the quad-pumped bus (See Fig. 9 and page 10, paragraph 115).

Greiner also teaches the parity data, interpreted as error code, being transmitted during a different cycle than the data (See page 10, paragraph 122, the eight line of the paragraph).

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
February 9, 2004

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